



# High Speed, Fast Settling Precision Operational Amplifier

## OP-42

### FEATURES

#### Fast

- Slew Rate ..... 50V/ $\mu$ s Min
- Settling-Time (0.01%) ..... 1 $\mu$ s Max
- Gain-Bandwidth Product ..... 10MHz Typ

#### Precise

- Common-Mode Rejection ..... 88dB Min
- Open-Loop Gain ..... 500V/mV Min
- Offset Voltage ..... 750 $\mu$ V Max
- Bias Current ..... 200pA Max

#### Excellent Radiation Hardness

Available in Die Form

### ORDERING INFORMATION <sup>†</sup>

| $T_A = 25^\circ\text{C}$ |         | PACKAGE      |               |          |                | OPERATING TEMPERATURE RANGE |  |
|--------------------------|---------|--------------|---------------|----------|----------------|-----------------------------|--|
| $V_{OS}$ MAX (mV)        | TO-99   | CERDIP 8-PIN | PLASTIC 8-PIN | SO 8-PIN | LCC 20-CONTACT |                             |  |
| 1.0                      | OP42AJ* | OP42AZ*      | —             | —        | OP42ARC/883    | MIL                         |  |
| 0.75                     | OP42EJ  | OP42EZ       | —             | —        | —              | IND                         |  |
| 1.5                      | OP42FJ  | OP42FZ       | —             | —        | —              | IND                         |  |
| 5.0                      | —       | —            | OP42GP        | OP42GS   | —              | XIND                        |  |

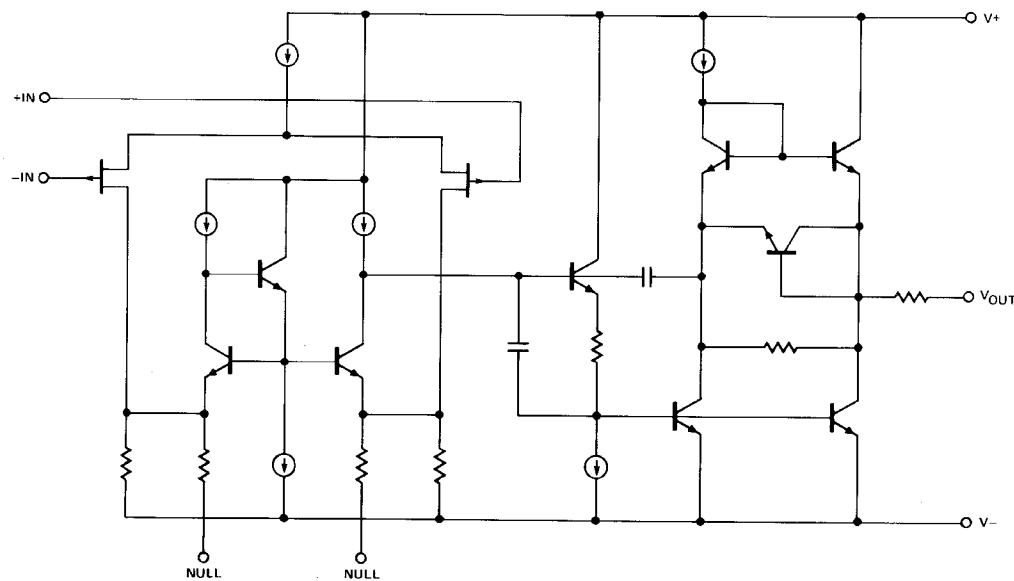
\* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages.

### GENERAL DESCRIPTION

The OP-42 is a fast precision JFET-input operational amplifier. Similar in speed to the OP-17, the OP-42 offers a symmetric

### SIMPLIFIED SCHEMATIC

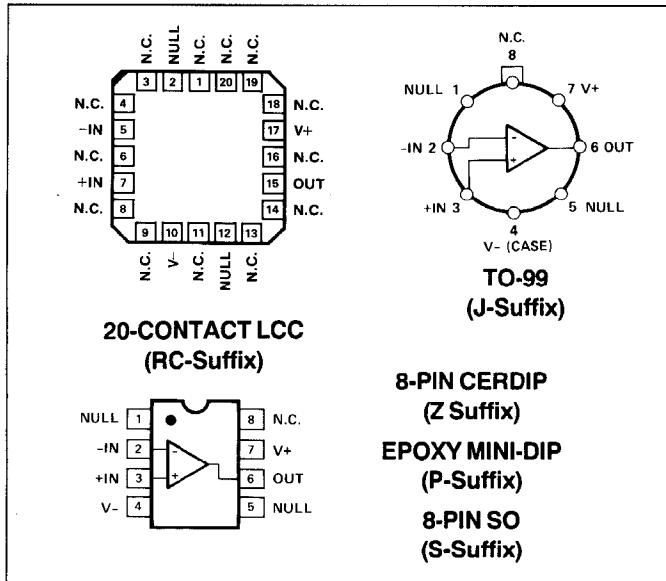


58V/ $\mu$ s slew rate and is internally compensated for unity-gain operation. OP-42 speed is achieved with a supply current of less than 6mA. Unity-gain stability, a wide full-power bandwidth of 900kHz, and a fast settling-time of 800ns to 0.01% make the OP-42 an ideal output amplifier for fast digital-to-analog converters.

Equal attention was given to both speed and precision in the OP-42 design. Its tight 750 $\mu$ V maximum input offset voltage combined with well-controlled drift of less than 10 $\mu$ V/ $^\circ\text{C}$  eliminates the need for external nulling in many circuits. The OP-42's

*Continued*

### PIN CONNECTIONS



# OP-42

## GENERAL DESCRIPTION *Continued*

common-mode rejection of 88dB minimum over a  $\pm 11V$  input voltage range is exceptional for a high-speed amplifier. High CMR combined with a minimum 500V/mV gain into  $10k\Omega$  load ensure excellent linearity in both noninverting and inverting gain configurations. The low input bias and offset currents provided by the JFET input stage suit the OP-42 for use in high-speed sample and hold circuits, peak detectors, and log amplifiers. Excellent radiation hardness characteristics make the OP-42 ideal for military and aerospace applications.

The OP-42 conforms to the standard 741 pinout with nulling to  $V_-$ . The OP-42 upgrades the performance of circuits using the AD544, AD611, AD711, and LF400 by direct replacement. In circuits without nulling, the OP-42 offers an upgrade for designs using the OP-16, OP-17, LT1022, LT1056, and HA2510.

## ABSOLUTE MAXIMUM RATINGS (Note 1)

|                                     |           |
|-------------------------------------|-----------|
| Supply Voltage                      | $\pm 20V$ |
| Input Voltage (Note 2)              | $\pm 20V$ |
| Differential Input Voltage (Note 2) | 40V       |
| Output Short-Circuit Duration       | Indefined |

ELECTRICAL CHARACTERISTICS at  $V_S = \pm 15V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

| PARAMETER                        | SYMBOL    | CONDITIONS  | OP-42E                                |                   |                   | OP-42F     |                   |                   | OP-42G     |                   |                   | UNITS     |
|----------------------------------|-----------|---|---------------------------------------|-------------------|-------------------|------------|-------------------|-------------------|------------|-------------------|-------------------|-----------|
|                                  |           |   | MIN                                   | TYP               | MAX               | MIN        | TYP               | MAX               | MIN        | TYP               | MAX               |           |
| Offset Voltage                   | $V_{OS}$  |   | —                                     | 0.3               | 0.75              | —          | 0.4               | 1.5               | —          | 1.5               | 5.0               | mV        |
| Input Bias Current               | $I_B$     | $V_{CM} = 0V$ $T_J = 25^\circ C$                          | —                                     | 80                | 200               | —          | 130               | 250               | —          | 130               | 250               | pA        |
| Input Offset Current             | $I_{OS}$  | $V_{CM} = 0V$ $T_J = 25^\circ C$                          | —                                     | 4                 | 40                | —          | 6                 | 50                | —          | 6                 | 50                | pA        |
| Input Voltage Range              | IVR       | (Note 1)  | $\pm 11$                              | +12.5<br>-12.0    | —                 | $\pm 11$   | +12.5<br>-12.0    | —                 | $\pm 11$   | +12.5<br>-12.0    | —                 | V         |
| Common-Mode Rejection            | CMR       | $V_{CM} = \pm 11V$  | 88                                    | 98                | —                 | 80         | 92                | —                 | 80         | 92                | —                 | dB        |
| Power-Supply Rejection Ratio     | PSRR      | $V_S = \pm 10V$<br>$\text{to } \pm 20V$                   | —                                     | 9                 | 40                | —          | 12                | 50                | —          | 12                | 50                | $\mu V/V$ |
| Large-Signal Voltage Gain        | $A_{VO}$  | $R_L = 10k\Omega$<br>$R_L = 2k\Omega$<br>$R_L = 1k\Omega$ | $V_O = \pm 10V$<br>$T_J = 25^\circ C$ | 500<br>200<br>100 | 900<br>260<br>170 | —          | 500<br>200<br>100 | 900<br>260<br>170 | —          | 500<br>200<br>100 | 900<br>260<br>170 | V/mV      |
| Output Voltage Swing             | $V_O$     | $R_L = 1k\Omega$  | $\pm 11.5$                            | +12.5<br>-11.9    | —                 | $\pm 11.5$ | +12.5<br>-11.9    | —                 | $\pm 11.5$ | +12.5<br>-11.9    | —                 | V         |
| Short-Circuit Current Limit      | $I_{SC}$  | Output Shorted to Ground                                  | $\pm 20$                              | +33<br>-28        | $\pm 60$          | $\pm 20$   | +33<br>-28        | $\pm 60$          | $\pm 20$   | +33<br>-28        | $\pm 60$          | mA        |
| Supply Current                   | $I_{SY}$  | No Load<br>$V_O = 0V$                                     | —                                     | 5.1               | 6.0               | —          | 5.1               | 6.5               | —          | 5.1               | 6.5               | mA        |
| Slew Rate                        | SR        |   | 50                                    | 58                | —                 | 40         | 50                | —                 | 40         | 50                | —                 | $V/\mu s$ |
| Full-Power Bandwidth             | $BW_p$    | (Note 2)  | 750                                   | 900               | —                 | 600        | 800               | —                 | 600        | 800               | —                 | kHz       |
| Gain-Bandwidth Product           | GBW       | $f_0 = 10\text{kHz}$                                      | —                                     | 10                | —                 | —          | 10                | —                 | —          | 10                | —                 | MHz       |
| Settling Time                    | $t_s$     | 10V Step 0.01% (Note 3)                                   | —                                     | 0.8               | 1.0               | —          | 0.9               | 1.2               | —          | 0.9               | 1.2               | $\mu s$   |
| Overload Recovery Time           | $t_{OR}$  |   | —                                     | 700               | —                 | —          | 700               | —                 | —          | 700               | —                 | ns        |
| Phase Margin                     | $\phi_o$  | 0db Gain  | —                                     | 47                | —                 | —          | 47                | —                 | —          | 47                | —                 | degrees   |
| Gain Margin                      | $A_{180}$ | 180° Open-Loop Phase Shift                                | —                                     | 9                 | —                 | —          | 9                 | —                 | —          | 9                 | —                 | dB        |
| Capacitive Load Drive Capability | $C_L$     | Unity-Gain Stable (Note 4)                                | 100                                   | 300               | —                 | 100        | 300               | —                 | 100        | 300               | —                 | pF        |

ELECTRICAL CHARACTERISTICS at  $V_S = \pm 15V$ ,  $T_A = +25^\circ C$ , unless otherwise noted. *Continued*

| PARAMETER                    | SYMBOL    | CONDITIONS            | OP-42E  |              |          | OP-42F  |              |          | OP-42G  |              |          | UNITS           |
|------------------------------|-----------|-----------------------|---------|--------------|----------|---------|--------------|----------|---------|--------------|----------|-----------------|
|                              |           |                       | MIN     | TYP          | MAX      | MIN     | TYP          | MAX      | MIN     | TYP          | MAX      |                 |
| Differential Input Impedance | $Z_{IN}$  |                       | —       | $10^{12}  6$ | —        | —       | $10^{12}  6$ | —        | —       | $10^{12}  6$ | —        | $\Omega  \mu F$ |
| Open-Loop Output Resistance  | $R_O$     |                       | —       | 50           | —        | —       | 50           | —        | —       | 50           | —        | $\Omega$        |
| Voltage Noise                | $e_n$ p-p | 0.1Hz to 10Hz         | —       | 2            | —        | —       | 2            | —        | —       | 2            | —        | $\mu V$ p-p     |
| Voltage Noise Density        | $e_n$     | $f_O = 10Hz$          | —       | 38           | —        | —       | 38           | —        | —       | 38           | —        |                 |
|                              |           | $f_O = 100Hz$         | —       | 16           | —        | —       | 16           | —        | —       | 16           | —        | nV/ $\sqrt{Hz}$ |
|                              |           | $f_O = 1kHz$          | —       | 13           | —        | —       | 13           | —        | —       | 13           | —        |                 |
|                              |           | $f_O = 10kHz$         | —       | 12           | —        | —       | 12           | —        | —       | 12           | —        |                 |
| Current Noise Density        | $i_n$     | $f_O = 1kHz$          | —       | 0.007        | —        | —       | 0.007        | —        | —       | 0.007        | —        | pA/ $\sqrt{Hz}$ |
| External $V_{OS}$ Trim Range |           | $R_{pot} = 20k\Omega$ | —       | 4            | —        | —       | 4            | —        | —       | 4            | —        | mV              |
| Long-Term $V_{OS}$ Drift     |           |                       | —       | 5            | —        | —       | 5            | —        | —       | 5            | —        | $\mu V/month$   |
| Supply Voltage Range         | $V_S$     |                       | $\pm 8$ | $\pm 15$     | $\pm 20$ | $\pm 8$ | $\pm 15$     | $\pm 20$ | $\pm 8$ | $\pm 15$     | $\pm 20$ | V               |

## NOTES:

1. Guaranteed by CMR test.

2. Guaranteed by slew-rate test and formula  $BW_p = SR/(2\pi 10V_{PEAK})$ .

3. Settling-time is sample tested for A and E grades. Test circuit is shown in Figure 4. Settling-time for F grade is guaranteed but not tested.

4. Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS at  $V_S = \pm 15V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

| PARAMETER                    | SYMBOL   | CONDITIONS                       | OP-42A     |                |          | UNITS      |
|------------------------------|----------|----------------------------------|------------|----------------|----------|------------|
|                              |          |                                  | MIN        | TYP            | MAX      |            |
| Offset Voltage               | $V_{OS}$ |                                  | —          | 0.3            | 1.0      | mV         |
| Input Bias Current           | $I_B$    | $V_{CM} = 0V$ $T_j = 25^\circ C$ | —          | 80             | 200      | pA         |
| Input Offset Current         | $I_{os}$ | $V_{CM} = 0V$ $T_j = 25^\circ C$ | —          | 4              | 40       | pA         |
| Input Voltage Range          | IVR      | (Note 1)                         | $\pm 11$   | +12.5<br>-12.0 | —        | V          |
| Common-Mode Rejection        | CMR      | $V_{CM} = \pm 11V$               | 86         | 96             | —        | dB         |
| Power-Supply Rejection Ratio | PSRR     | $V_S = \pm 10V$ to $\pm 20V$     | —          | 9              | 40       | $\mu V/V$  |
| Large-Signal Voltage Gain    | $A_{vo}$ | $R_L = 10k\Omega$                | 500        | 900            | —        |            |
|                              |          | $R_L = 2k\Omega$                 | 200        | 260            | —        | V/mV       |
|                              |          | $R_L = 1k\Omega$                 | 100        | 170            | —        |            |
| Output Voltage Swing         | $V_o$    | $R_L = 1k\Omega$                 | $\pm 11.5$ | +12.5<br>-11.9 | —        | V          |
| Short-Circuit Current Limit  | $I_{sc}$ | Output Shorted to Ground         | $\pm 20$   | +33<br>-28     | $\pm 60$ | mA         |
| Supply Current               | $I_{sy}$ | No Load $V_o = 0V$               | —          | 5.1            | 6.0      | mA         |
| Slew Rate                    | SR       |                                  | 45         | 52             | —        | V/ $\mu s$ |
| Full-Power Bandwidth         | $BW_p$   | (Note 2)                         | 700        | 850            | —        | kHz        |
| Gain-Bandwidth Product       | GBW      | $f_O = 10kHz$                    | —          | 10             | —        | MHz        |
| Settling Time                | $t_s$    | 10V Step 0.01% (Note 3)          | —          | 0.8            | 1.0      | $\mu s$    |
| Overload Recovery Time       | $t_{OR}$ |                                  | —          | 700            | —        | ns         |
| Phase Margin                 | $\phi_o$ | Odb Gain                         | —          | 47             | —        | degrees    |

# OP-42

**ELECTRICAL CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$ , unless otherwise noted. *Continued*

| PARAMETER                        | SYMBOL    | CONDITIONS   | MIN              | TYP                  | MAX              | UNITS           |
|----------------------------------|-----------|--|------------------|----------------------|------------------|-----------------|
| Gain Margin                      | $A_{180}$ | 180° Open-Loop Phase Shift                                     | —                | 9                    | —                | dB              |
| Capacitive Load Drive Capability | $C_L$     | Unity-Gain Stable (Note 4)                                     | 100              | 300                  | —                | pF              |
| Differential Input Impedance     | $Z_{IN}$  |  | —                | $10^{12}  6$         | —                | $\Omega  \mu F$ |
| Open-Loop Output Resistance      | $R_O$     |  | —                | 50                   | —                | $\Omega$        |
| Voltage Noise                    | $e_n$ p-p | 0.1Hz to 10Hz  | —                | 2                    | —                | $\mu V$ p-p     |
| Voltage Noise Density            | $e_n$     | $f_O = 10Hz$<br>$f_O = 100Hz$<br>$f_O = 1kHz$<br>$f_O = 10kHz$ | —<br>—<br>—<br>— | 38<br>16<br>13<br>12 | —<br>—<br>—<br>— | nV/ $\sqrt{Hz}$ |
| Current Noise Density            | $i_n$     | $f_O = 1kHz$   | —                | 0.007                | —                | pA/ $\sqrt{Hz}$ |
| External $V_{OS}$ Trim Range     |           | $R_{pot} = 20k\Omega$  | —                | 4                    | —                | mV              |
| Long-Term $V_{OS}$ Drift         |           |  | —                | 5                    | —                | $\mu V/month$   |
| Supply Voltage Range             | $V_S$     |  | $\pm 8$          | $\pm 15$             | $\pm 20$         | V               |

**NOTES:**

- Guaranteed by CMR test.
- Guaranteed by slew-rate test and formula  $BW_p = SR/(2\pi 10V_{PEAK})$ .
- Settling-time is sample tested for A and E grades. Test circuit is shown in Figure 4. Settling-time for F grade is guaranteed but not tested.
- Guaranteed but not tested.

**ELECTRICAL CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $-25^\circ C \leq T_A \leq 85^\circ C$  for E/F grades, and  $-40^\circ C \leq T_A \leq +85^\circ C$  for G grade, unless otherwise noted.

| PARAMETER                              | SYMBOL     | CONDITIONS   | OP-42E     |                |          | OP-42F     |                |          | OP-42G     |                |          |
|--|------------|--|------------|----------------|----------|------------|----------------|----------|------------|----------------|----------|
|  |            |  | MIN        | TYP            | MAX      | MIN        | TYP            | MAX      | MIN        | TYP            | MAX      |
| Offset Voltage                         | $V_{OS}$   |  | —          | 0.4            | 1.2      | —          | 0.6            | 2.5      | —          | 2.0            | 6.0      |
| Offset Voltage Temperature Coefficient | $TCV_{OS}$ |  | —          | 4              | 10       | —          | 8              | —        | —          | 8              | —        |
| Input Bias Current                     | $I_B$      | (Note 1)   | —          | 0.5            | 1.2      | —          | 0.6            | 2.0      | —          | 0.6            | 2.0      |
| Input Offset Current                   | $I_{OS}$   | (Note 1)   | —          | 0.05           | 0.2      | —          | 0.06           | 0.4      | —          | 0.06           | 0.4      |
| Input Voltage Range                    | $IVR$      | (Note 2)   | $\pm 11$   | +12.5<br>—12.0 | —        | $\pm 11$   | +12.5<br>—12.0 | —        | $\pm 11$   | +12.5<br>—12.0 | —        |
| Common-Mode Rejection                  | CMR        | $V_{CM} = \pm 11V$   | 86         | 96             | —        | 80         | 94             | —        | 80         | 94             | —        |
| Power-Supply Rejection Ratio           | PSRR       | $V_S = \pm 10V$ to $\pm 20V$                                   | —          | 2              | 40       | —          | 6              | 50       | —          | 6              | 50       |
| Large-Signal Voltage Gain              | $A_{VO}$   | $R_L = 10k\Omega$ (Note 1)<br>$R_L = 2k\Omega$ $V_O = \pm 10V$ | 200<br>100 | 500<br>160     | —        | 200<br>100 | 500<br>160     | —        | 200<br>100 | 500<br>160     | —        |
| Output Voltage Swing                   | $V_O$      | $R_L = 2k\Omega$   | $\pm 11.0$ | +12.3<br>—11.8 | —        | $\pm 11.0$ | +12.3<br>—11.8 | —        | $\pm 11.0$ | +12.3<br>—11.8 | —        |
| Short-Circuit Current Limit            | $I_{SC}$   | Output Shorted to Ground                                       | $\pm 8$    | —              | $\pm 60$ | $\pm 8$    | —              | $\pm 60$ | $\pm 8$    | —              | $\pm 60$ |
| Supply Current                         | $I_{SY}$   | No Load $V_O = 0V$   | —          | 5.1            | 6.0      | —          | 5.1            | 6.5      | —          | 5.1            | 6.5      |
| Slew Rate                              | SR         | $R_L = 2k\Omega$   | 45         | 57             | —        | 40         | 50             | —        | 40         | 50             | —        |
| Capacitive Load Drive Capability       | $C_L$      | Unity-Gain Stable (Note 3)                                     | 100        | 250            | —        | 100        | 250            | —        | 100        | 250            | —        |

**NOTES:**

- $T_j = 85^\circ C$  for E/F/G Grades;  $T_j = 125^\circ C$  for A grade.

- Guaranteed by CMR test.

- Guaranteed but not tested.

**ELECTRICAL CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $-55^\circ C \leq T_A \leq 125^\circ C$  for A grade, unless otherwise noted.

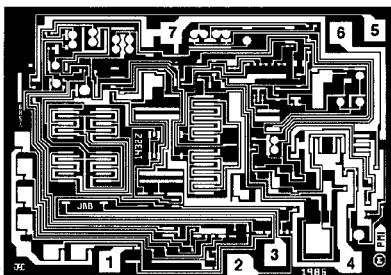
| PARAMETER                                    | SYMBOL     | CONDITIONS   | OP-42A     |                |          |                   |
|--|------------|--|------------|----------------|----------|-------------------|
|  |            |  | MIN        | TYP            | MAX      |                   |
| Offset Voltage                               | $V_{OS}$   |  | —          | 0.5            | 2.0      | mV                |
| Offset Voltage<br>Temperature<br>Coefficient | $TCV_{OS}$ |  | —          | 4              | 10       | $\mu V/^{\circ}C$ |
| Input Bias Current                           | $I_B$      | (Note 1)   | —          | 6              | 20       | nA                |
| Input Offset Current                         | $I_{OS}$   | (Note 1)   | —          | 0.2            | 1.0      | nA                |
| Input Voltage Range                          | IVR        | (Note 2)   | $\pm 11$   | +12.5<br>-12.0 | —        | V                 |
| Common-Mode<br>Rejection                     | CMR        | $V_{CM} = \pm 11V$   | 80         | 94             | —        | dB                |
| Power-Supply<br>Rejection Ratio              | PSRR       | $V_S = \pm 10V$<br>to $\pm 20V$                                | —          | 10             | 50       | $\mu V/V$         |
| Large-Signal<br>Voltage Gain                 | $A_{VO}$   | $R_L = 10k\Omega$ (Note 1)<br>$R_L = 2k\Omega$ $V_O = \pm 10V$ | 160<br>80  | 350<br>110     | —        | $V/mV$            |
| Output Voltage<br>Swing                      | $V_O$      | $R_L = 2k\Omega$   | $\pm 11.0$ | +12.3<br>-11.8 | —        | V                 |
| Short-Circuit<br>Current Limit               | $I_{SC}$   | Output Shorted<br>to Ground                                    | $\pm 8$    | —              | $\pm 60$ | mA                |
| Supply Current                               | $I_{SY}$   | No Load<br>$V_O = 0V$  | —          | 5.1            | 6.0      | mA                |
| Slew Rate                                    | SR         | $R_L = 2k\Omega$   | 40         | 52             | —        | $V/\mu s$         |
| Capacitive Load<br>Drive Capability          | $C_L$      | Unity-Gain Stable<br>(Note 3)                                  | 100        | 250            | —        | pF                |

**NOTES:**

1.  $T_j = 85^\circ C$  for E/F Grades;  $T_j = 125^\circ C$  for A grade.
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

# OP-42

## DICE CHARACTERISTICS



1. OFFSET VOLTAGE NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. NEGATIVE SUPPLY
5. OFFSET VOLTAGE NULL
6. AMPLIFIER OUTPUT
7. POSITIVE SUPPLY

DIE SIZE 0.098 × 0.070 inch, 6860 sq. mils  
(2.49 × 1.78 mm, 4.43 sq. mm)

WAFER TEST LIMITS at  $V_S = \pm 15V$ ,  $T_j = 25^\circ C$ , unless otherwise noted.

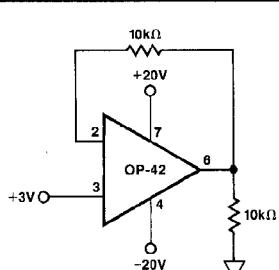
| PARAMETER                        | SYMBOL   | CONDITIONS                    | OP-42N<br>LIMIT | UNITS         |
|----------------------------------|----------|-------------------------------|-----------------|---------------|
| Offset Voltage                   | $V_{OS}$ |                               | 1.5             | mV MAX        |
| Input Bias Current               | $I_B$    | $V_{CM} = 0V$                 | 250             | pA MAX        |
| Input Offset Current             | $I_{OS}$ | $V_{CM} = 0V$                 | 50              | pA MAX        |
| Input Voltage Range              | IVR      | (Note 1)                      | $\pm 11$        | V MIN         |
| Common-Mode Rejection            | CMR      | $V_{CM} = \pm 11V$            | 80              | dB MIN        |
| Power-Supply Rejection Ratio     | PSRR     | $V_S = \pm 10V$ to $\pm 20V$  | 50              | $\mu V/V$ MAX |
| Large-Signal Voltage Gain        | $A_{VO}$ | $R_L = 10k\Omega$             | 500             | V/mV MIN      |
|                                  |          | $R_L = 2k\Omega$              | 200             |               |
|                                  |          | $R_L = 1k\Omega$              | 100             |               |
| Output Voltage Swing             | $V_O$    | $R_L = 1k\Omega$              | $\pm 11.5$      | V MIN         |
| Short-Circuit Current Limit      | $I_{SC}$ | Output Shorted to Ground      | $\pm 20/\pm 60$ | mA MIN/MAX    |
| Supply Current                   | $I_{SY}$ | No Load<br>$V_O = 0V$         | 6.5             | mA MAX        |
| Slew Rate                        | SR       |                               | 40              | $V/\mu s$ MIN |
| Capacitive Load Drive Capability | $C_L$    | Unity-Gain Stable<br>(Note 2) | 100             | pF MIN        |

### NOTES:

1. Guaranteed by CMR test.
2. Guaranteed but not tested.

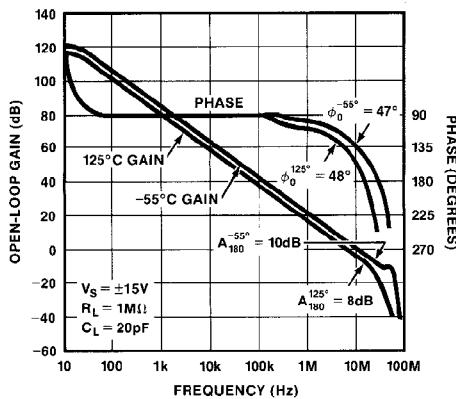
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

## BURN-IN CIRCUIT

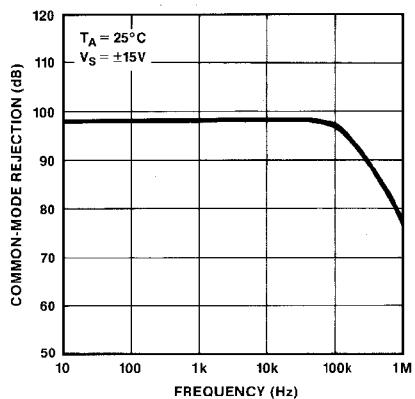


## TYPICAL PERFORMANCE CHARACTERISTICS

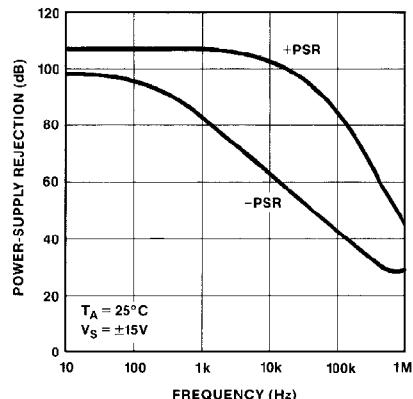
OPEN-LOOP GAIN, PHASE vs FREQUENCY



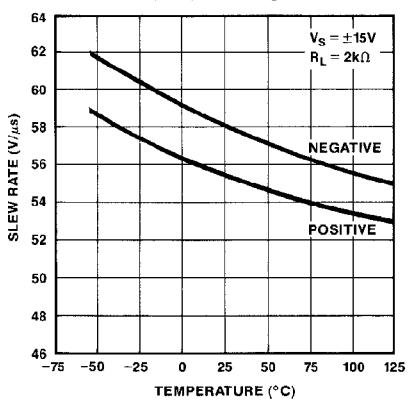
COMMON-MODE REJECTION vs FREQUENCY



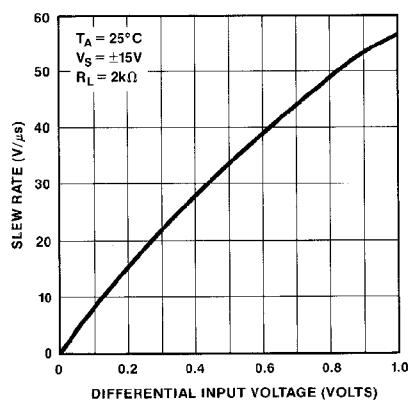
POWER-SUPPLY REJECTION vs FREQUENCY



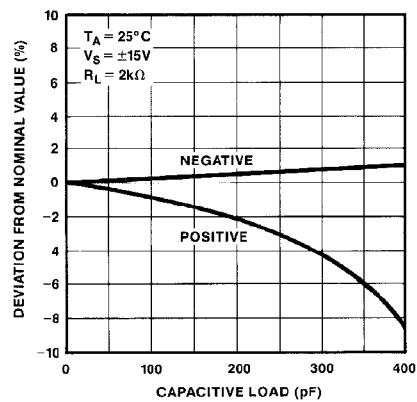
SLEW RATE vs TEMPERATURE



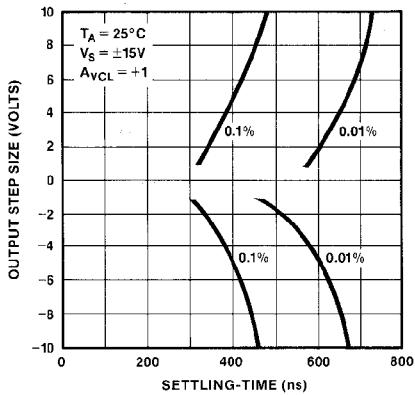
SLEW RATE vs DIFFERENTIAL INPUT VOLTAGE



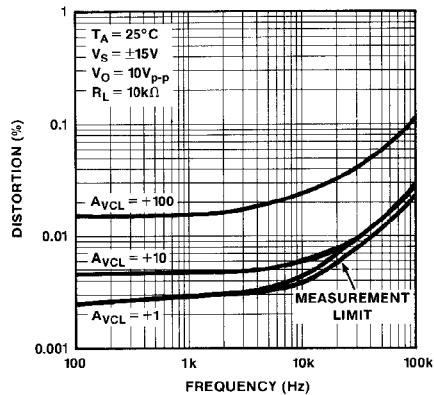
SLEW RATE vs CAPACITIVE LOAD



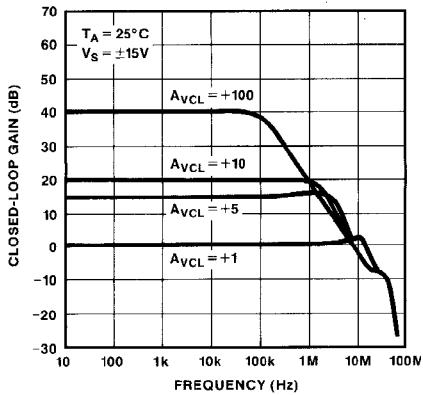
SETTLING-TIME vs STEP SIZE



DISTORTION vs FREQUENCY

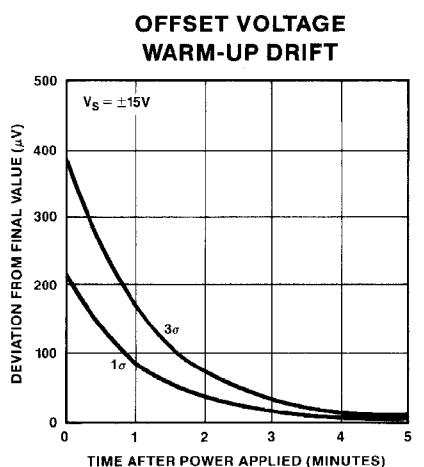
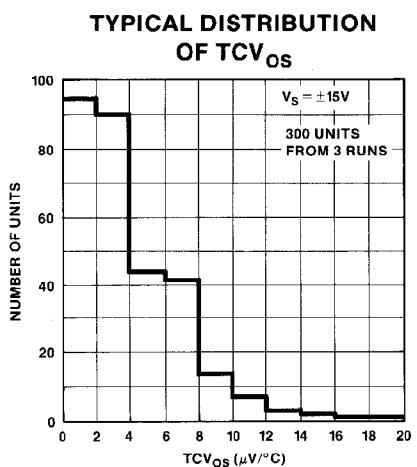
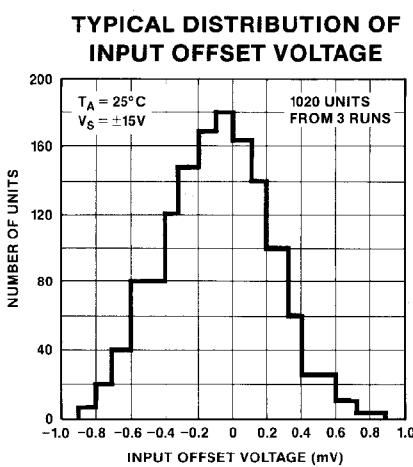
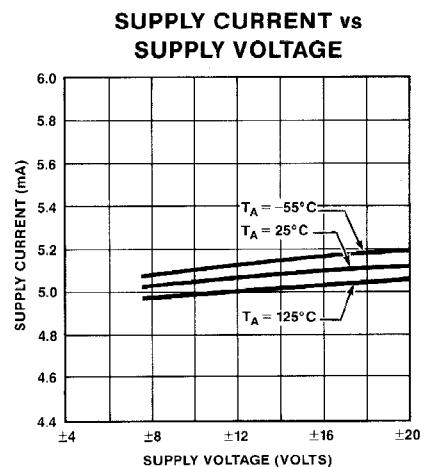
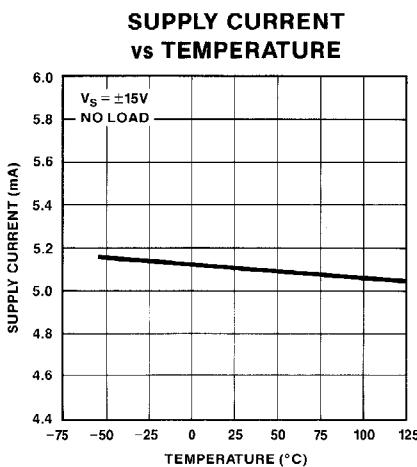
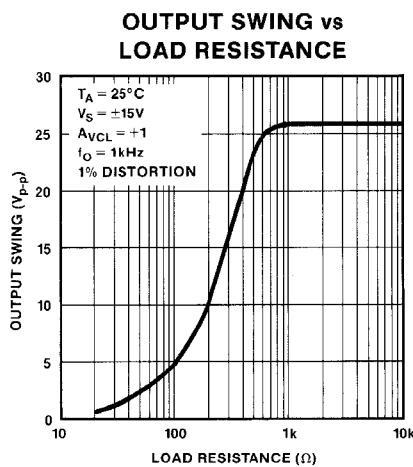
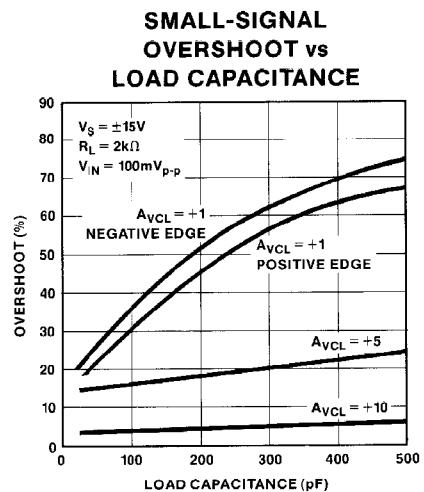
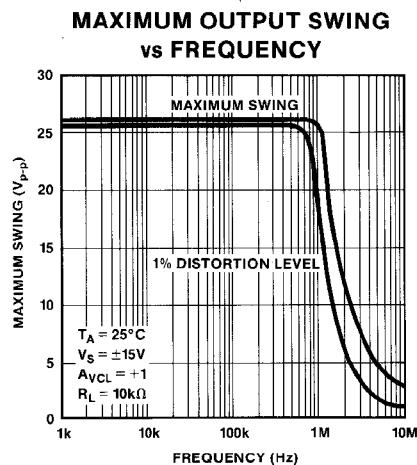
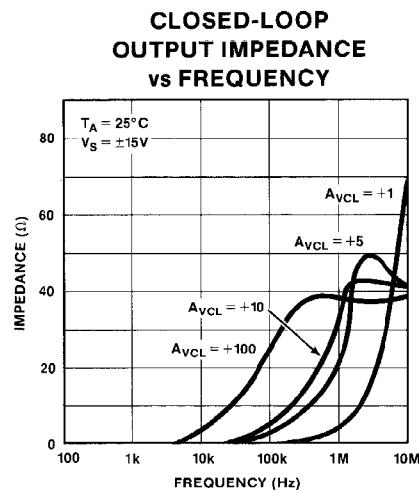


CLOSED-LOOP GAIN vs FREQUENCY

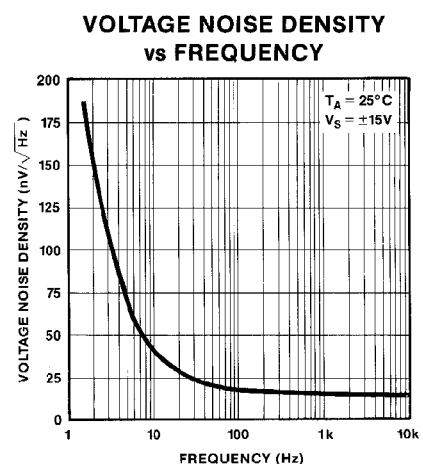
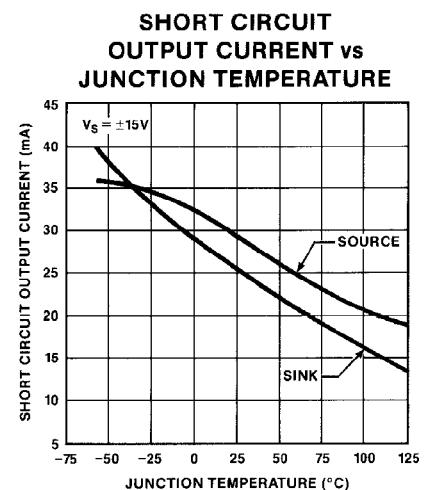
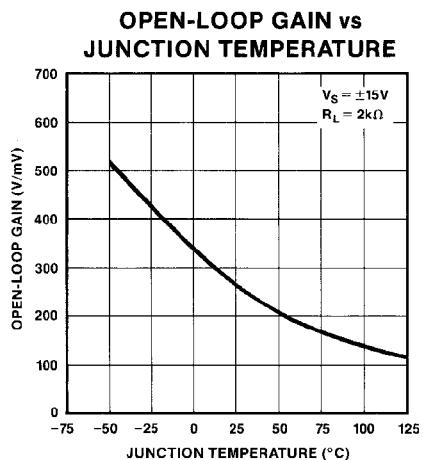
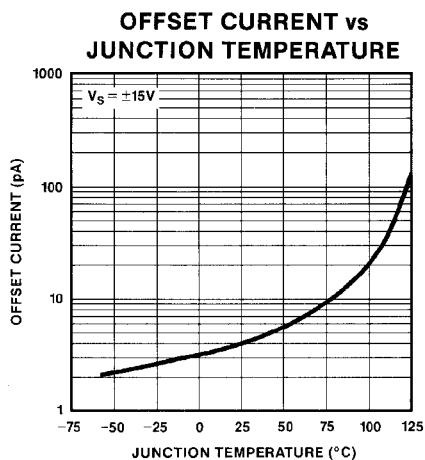
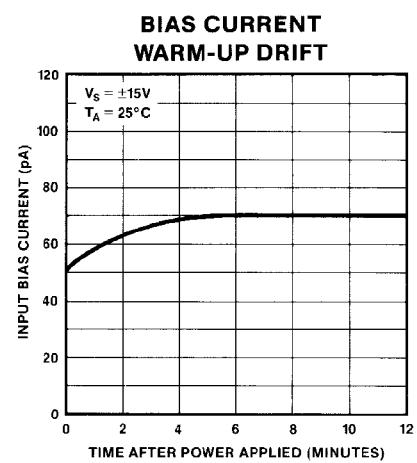
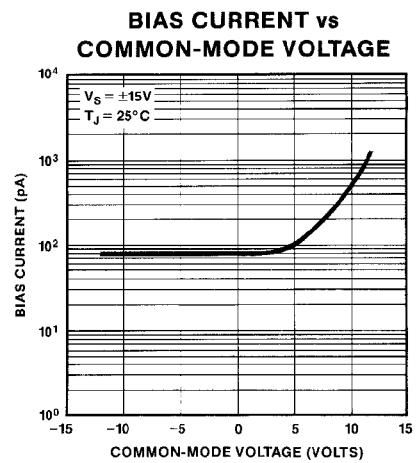
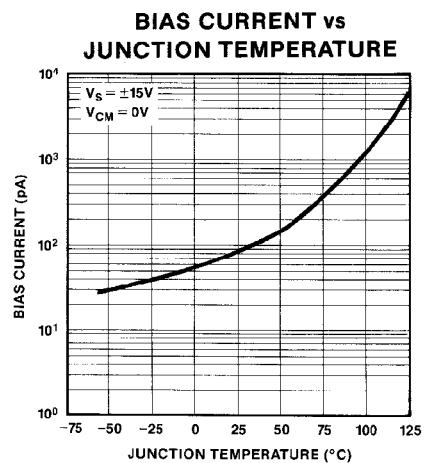


# OP-42

## TYPICAL PERFORMANCE CHARACTERISTICS



## TYPICAL PERFORMANCE CHARACTERISTICS

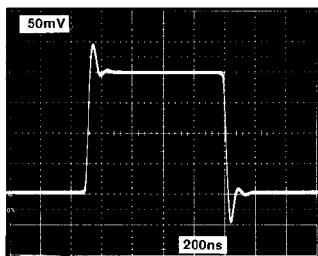


# OP-42

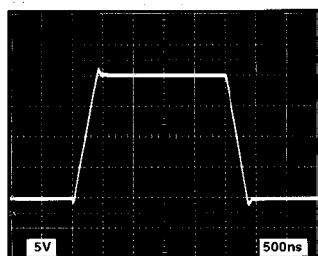
## APPLICATIONS INFORMATION

The OP-42 combines speed with a high level of input precision usually found only with slower devices. Well-behaved AC performance in the form of clean transient response, symmetrical slew-rates and a high degree of forgiveness to supply decoupling are the hallmarks of this amplifier. AC gain and phase response are quite independent of temperature or supply voltage. Figure 1 shows the OP-42's small-signal response. Even with 75pF loads, there is minimal ringing in the output waveform. Large-signal response is shown in Figure 2. This figure clearly shows the OP-42's exceptionally close matching between positive and negative slew-rates. Slew-rate symmetry decreases the DC offset a system encounters when processing high-frequency signals, and thus reduces the DC current necessary for load driving.

**FIGURE 1:** Small-Signal Transient Response,  
 $Z_L = 2\text{k}\Omega \parallel 75\text{pF}$



**FIGURE 2:** Large-Signal Transient Response,  
 $Z_L = 2\text{k}\Omega \parallel 75\text{pF}$



As with most JFET-input amplifiers, the output of the OP-42 may undergo phase inversion if either input exceeds the specified input voltage range. Phase inversion will not damage the amplifier, nor will it cause an internal latch-up.

Supply decoupling should be used to overcome inductance and resistance associated with supply lines to the amplifier.

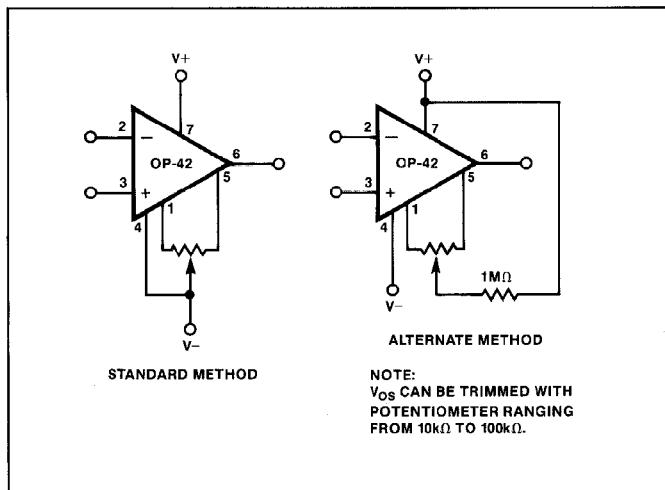
For most applications a  $0.1\mu\text{F}$  to  $0.01\mu\text{F}$  capacitor should be placed between each supply pin and ground.

The OP-42 displays excellent resistance to radiation. Radiation hardness data is available by contacting the factory.

## OFFSET VOLTAGE ADJUSTMENT

Offset voltage is adjusted with a  $10\text{k}\Omega$  to  $100\text{k}\Omega$  potentiometer as shown in Figure 3. The potentiometer should be connected between pins 1 and 5 with its wiper connected to the  $V_+$  supply. Nulling  $V_{OS}$  in this manner changes  $TCV_{OS}$  by no more than  $5\mu\text{V}/^\circ\text{C}$  per millivolt of  $V_{OS}$  change. Alternately,  $V_{OS}$  may be nulled by attaching the potentiometer wiper through a  $1\text{M}\Omega$  resistor to the positive supply rail.

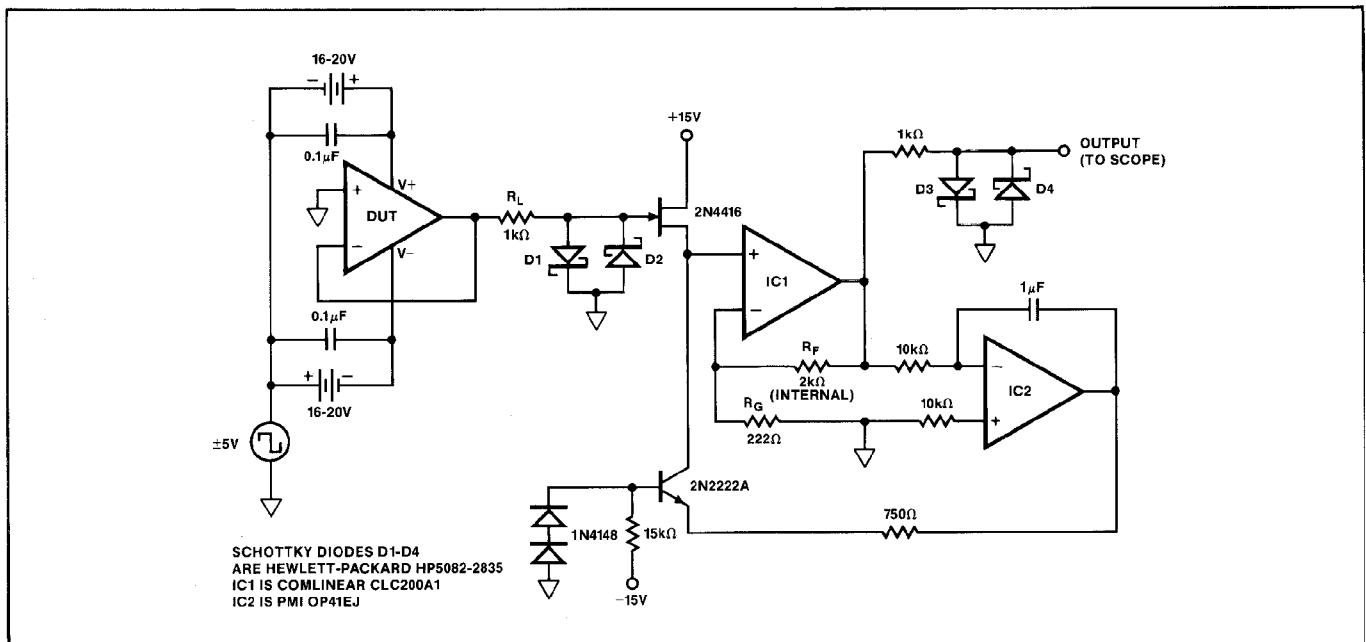
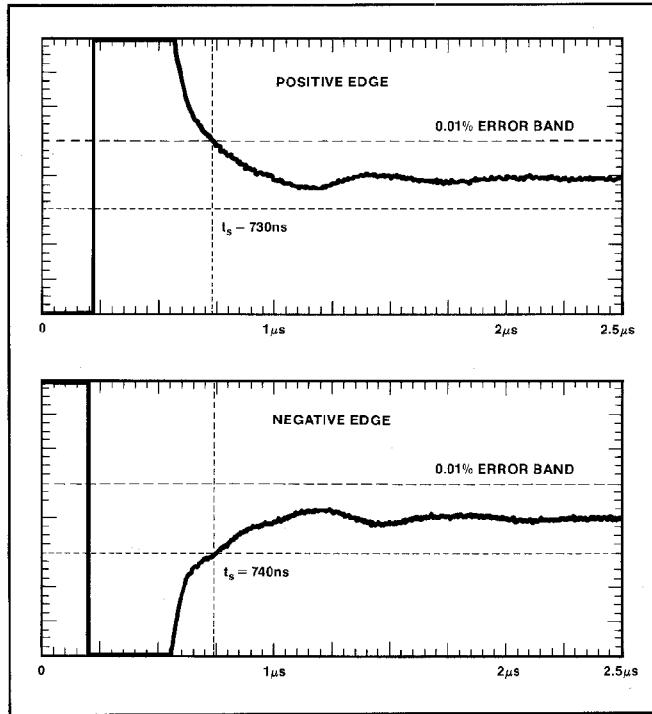
**FIGURE 3:** Input Offset Voltage Nulling



## SETTLING-TIME

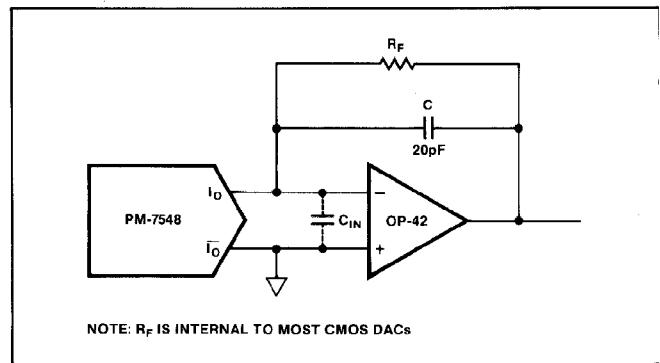
Guaranteed fast-settling is assured by sample-testing during production. The OP-42 is configured as a unity-gain follower in the test circuit of Figure 4. This test method has advantages over false-sum-node techniques in that the actual output of the amplifier is measured, instead of an error-voltage at the sum node. Common-mode settling effects are exercised in this circuit, in addition to the slew-rate and bandwidth effects measured by the false-sum-node method. A reasonably flat-top pulse is required as a stimulus.

The output waveform of the OP-42 being tested is clamped by Schottky diodes and buffered by the JFET source-follower. The signal is amplified by a factor of ten by the fast amplifier IC1, then Schottky-clamped before being output. The OP-41 provides overall offset nulling. Analysis of the waveform using a digitizing oscilloscope determines the op amp's settling-time.

**FIGURE 4:** Settling-Time Test Fixture**FIGURE 5:** OP-42 Settling-Characteristics**DAC OUTPUT AMPLIFIER**

The OP-42 is an excellent choice for a DAC output amplifier, since its high speed and fast settling-time allow quick transitions between codes, even for full-scale changes in output level. The DAC output capacitance appears at the operational amplifier inputs, and must be compensated to ensure

optimal settling speed. Compensation is achieved with capacitor C in Figure 6. C must be adjusted to account for the DAC's output capacitance, the op amp's input capacitance, and any stray capacitance at the inputs. With a bipolar DAC, an additional shunt resistor may be used to optimize response. This technique is described in PMI's application note AN-24.

**FIGURE 6:** DAC Output Amplifier Circuit

Highest speed is achieved using bipolar DACs such as PMI's DAC-08, DAC-10 or DAC-312. The output capacitances of these converters are up to an order of magnitude lower than their CMOS counterparts, resulting in substantially faster settling-times. The high output impedance of bipolar DACs allows the output amplifier to operate in a true current-to-voltage mode, with a noise gain of unity, thereby retaining the amplifier's full bandwidth. Offset voltage has minimal effect on linearity with bipolar converters.

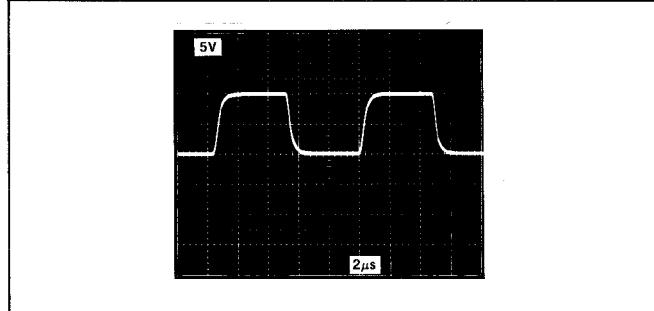
CMOS digital-to-analog converters have higher output capacitances and lower output resistances than bipolar DACs.

OP-42

This results in slower settling-times, higher sensitivity to offset voltages and a reduction in the output amplifier's bandwidth. These trade-offs must be balanced against the CMOS DAC's advantages in terms of interfacing capability, power dissipation, accuracy levels and cost. Using the internal feedback resistor which is present on most CMOS converters, the gain applied to offset voltage varies between 4/3 and 2, depending upon output code. Contributions to linearity error will be as much as  $2/3V_{OS}$ . In a 10-volt 12-bit system, this may add up to an additional 1/5LSB DNL with the OP-42E. Amplifier bandwidth is reduced by the same gain factor applied to offset voltage, however the OP-42's 10MHz gain-bandwidth product results in no reduction of the CMOS converter's multiplying bandwidth.

Individual DAC data-sheets should be consulted for more complete descriptions of the converters and their circuit applications.

**FIGURE 7:** DAC Output Amplifier Response (PM-7545 DAC)



## DRIVING A HIGH-SPEED ADC

The OP-42's open-loop output resistance is approximately  $50\Omega$ . When feedback is applied around the amplifier, output resistance decreases in proportion to open-loop gain divided by closed-loop gain ( $A_{vOL}/A_{vCL}$ ). Output impedance increases as open-loop gain rolls-off with frequency. High-speed analog-to-digital converters require low source impedances at high frequency. Output impedance at 1MHz is typically  $5\Omega$  for an OP-42 operating at unity-gain. If lower output impedances are required, an output buffer may be placed at the output of the OP-42.

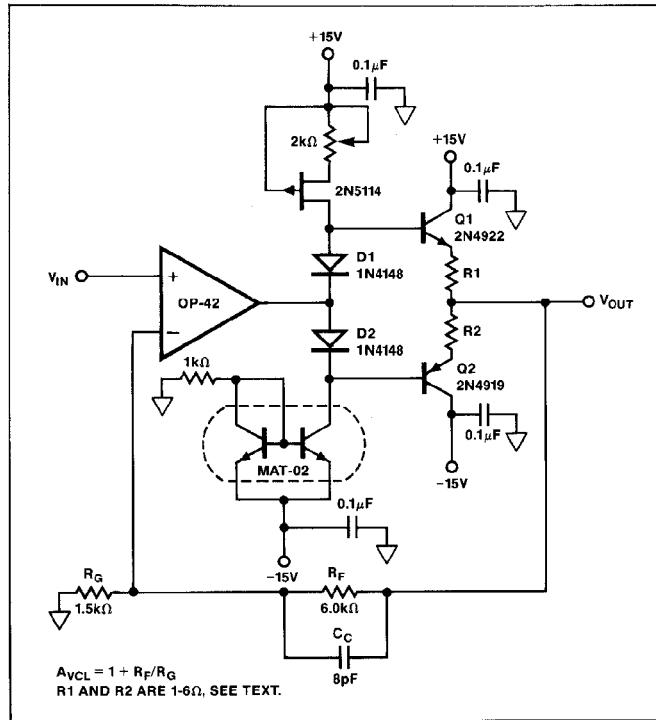
## HIGH-CURRENT OUTPUT BUFFER

The circuit in Figure 8 shows a high-current output stage for the OP-42. Output current is limited by R1 and R2. For good tracking between the output transistors Q1, Q2 and their biasing diodes D1 and D2, thermal contact must be maintained between the transistor and its associated diode. If good thermal contact is not maintained, R1 and R2 must be increased to 5-6 $\Omega$  in order to prevent thermal runaway. Using 5 $\Omega$  resistors, the circuit easily drives a 75 $\Omega$  load (Figure 9). Output resistance is decreased and heavier loads may be driven by decreasing R1 and R2.

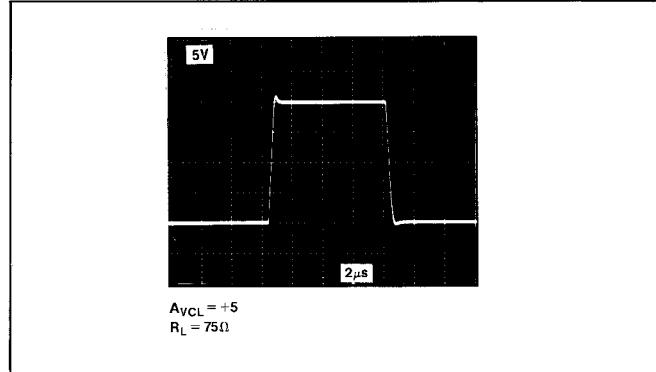
Base current and biasing for Q1 and Q2 are provided by two current sources, the MAT-02 and the JFET. The  $2k\Omega$  potentiometer in the JFET current source should be trimmed for optimum transient performance. The case of the MAT-02 should be connected to V<sub>-</sub>, and decoupled to ground with a

0.1 $\mu$ F capacitor. Compensation for the OP-42's input capacitance is provided by  $C_C$ . The circuit may be operated at any gain, in the usual op amp configurations.

**FIGURE 8:** High-Current Output Buffer



**FIGURE 9:** Output Buffer Large-Signal Response



## **DRIVING CAPACITIVE LOADS**

Best performance will always be achieved by minimizing input and load capacitances around any high-speed amplifier. However, the OP-42 is guaranteed capable of driving a 100pF capacitive load over its full operating temperature range while operating at any gain including unity. Typically, an OP-42 will drive more than 250pF at any temperature. Supply decoupling does affect capacitive load driving ability. Extra care should be given to ensure good decoupling when driving capacitive loads, and a larger decoupling capacitor between  $1\mu\text{F}$  and  $10\mu\text{F}$  should be placed in parallel with the usual decoupling capacitor on each supply.

Large capacitive loads may be driven utilizing the circuit shown in Figure 10. R1 and C1 introduce a small amount of feedforward compensation around the amplifier to counteract the phase lag induced by the output impedance and load capacitance. At DC and low frequencies, R1 is contained within the feedback loop. At higher frequencies, feedforward compensation becomes increasingly dominant, and R1's effect on output impedance will become more noticeable.

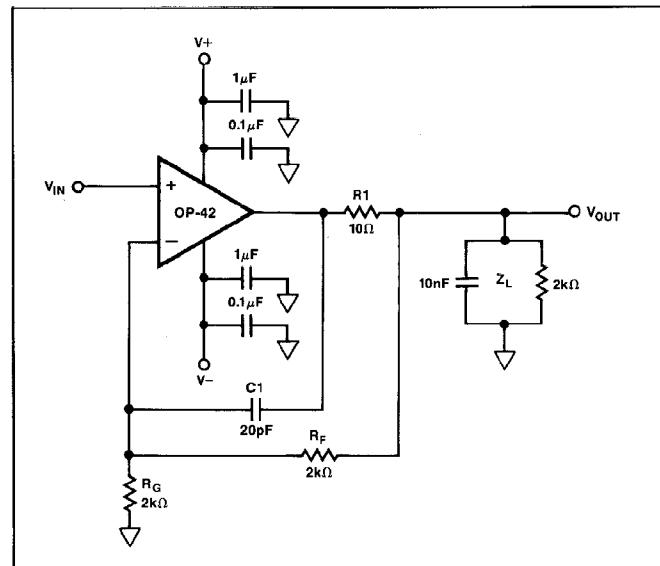
When driving very large capacitances, slew-rate will be limited by the short-circuit current limit. Although the unloaded slew-rate is insensitive to variations in temperature, the output current limit has a negative temperature coefficient, and is asymmetrical with regards to sourcing and sinking current. Therefore, slew-rate into excessive capacities will decrease with increasing temperature, and will lose symmetry.

## **COMPUTER SIMULATIONS**

Many electronic design and analysis programs include models for op amps which calculate AC performance from the location of poles and zeros. As an aid to designers utilizing such a program, major poles and zeros of the OP-42 are listed below. Their location will vary slightly between production lots. Typically, they will be within  $\pm 15\%$  of the frequency listed. Use of this data will enable the designer to evaluate gross circuit performance quickly, but should not supplant rigorous characterization of a breadboarded circuit.

| POLES  | ZEROS |
|--------|-------|
| 20Hz   | 1MHz  |
| 300kHz |       |
| 3MHz   |       |

**FIGURE 11:** OP-41 Servo Amplifier Provides Offset Correction

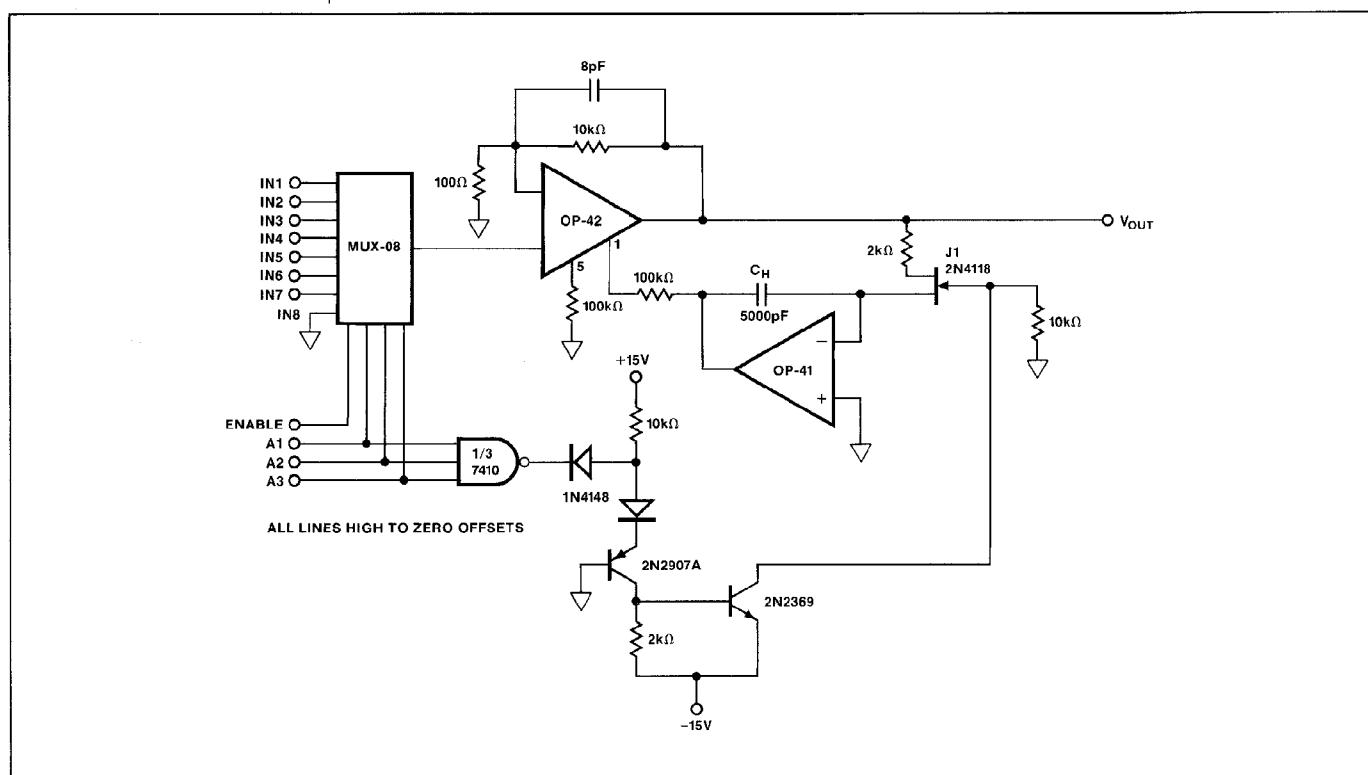


## AUTOZEROING OFFSET VOLTAGE

Figure 11 describes a circuit for automatic offset voltage and drift correction. The OP-41 is used in a servo loop to force the OP-42 output equal to the OP-41's offset voltage. Thus, the OP-42's effective input offset is held below  $10\mu V$  ( $1mV/A \cdot V_{CL} = 100$ ) despite any temperature variations. This circuit will be most advantageous in high-gain applications.

Feedback is accomplished using the OP-42's null pins, leaving both inputs free for other purposes. In the application

**FIGURE 11:** OP-41 Servo Amplifier Provides Offset Correction



## OP-42

shown, the OP-42 has seven multiplexed inputs, while the eighth input provides a ground reference. Nulling is accomplished by addressing the grounded channel. This address should be held for at least 200 $\mu$ s. After this time, the address may be changed to another channel. The MUX-08 ENABLE pin must be high during the entire nulling cycle. During this time, JFET switch J1 turns on, completing feedback around

the OP-41 servo amplifier. A charge is developed across  $C_H$  to compensate for the OP-42's offset voltage. When another channel is addressed, J1 turns off, and the correction charge is maintained across  $C_H$  by the OP-41. Droop is exceptionally low — only 1.3 $\mu$ V/s at 25°C. A correction range of more than 4mV allows nulling of minor system offsets as well as the OP-42's offset voltage.